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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/593,713	09/21/2006	Genichi Fujiwara	295586US2PCT	3113
22850 7590 06/19/2009 OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			EXAMINER GUARINO, RAHEL	
			ART UNIT	PAPER NUMBER
			2611	
			NOTIFICATION DATE	DELIVERY MODE
			06/19/2009	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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<b>Office Action Summary</b>	<b>Application No.</b> 10/593,713	<b>Applicant(s)</b> FUJIWARA, GENICHI	
	<b>Examiner</b> Rahel Guarino	<b>Art Unit</b> 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 21 September 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-11 is/are rejected.
- 7) ☒ Claim(s) 3 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### *Specification*

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

**The abstract should be in narrative** form and generally limited to a single paragraph on a separate sheet within the **range of 50 to 150 words**. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The abstract of the disclosure is objected to because it is **over 150 words**.

Correction is required. See MPEP § 608.01(b).

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1,2,4,6-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nogawa US 6,154,071 in view of Chang et al. US 6,642,769

Re claim 1, Nogawa discloses a phase locked loop (PLL) circuit comprising (fig.4): a phase comparator (101) that receives a reference clock signal and a comparison clock signal, compares a phase of the reference clock signal with a phase of the comparison clock signal (col. 6 lines 19-25), produces a rectangular wave signal having three voltage levels corresponding to phase differences (fig.5; col. 7 lines 39-50, lag/lead and constant), and outputs the rectangular wave signal (fig.5); a voltage controlled oscillator (VCO, 106) that receives the rectangular wave signal outputted from the level shifter, and outputs a clock signal whose frequency corresponds to the voltage level of the rectangular wave signal; and a frequency divider (107) that divides the frequency of the clock signal outputted from the VCO by N (N is a counting number) (col. 13 lines 14-17), and feeds back a signal whose frequency is divided to the phase comparator as the comparison clock signal (fig.4 shows feeding back "*signal to be compared*" as input to the a phase comparator (101); col. 6 lines 21-25)); does not teach a level shifter that receives the rectangular wave signal outputted from the phase comparator, shifts a voltage level of the rectangular wave signal, and outputs the rectangular wave signal whose voltage level has been shifted.

However, Chang discloses a level shifter (3) that receives the rectangular wave (fig.4) signal outputted from the phase comparator (Nogawa's phase comparator), shifts a voltage level of the rectangular wave signal, and outputs the rectangular wave signal whose voltage level has been shifted (fig.4 (output (col. 5 lines 1-12))).

Therefore, taking the combined teaching of Nogawa and Chang as a whole would have been rendered obvious to one skilled in the art to modify Nogawa to utilize a level shifter that receives the rectangular wave signal outputted from the phase comparator, shifts a voltage level of the rectangular wave signal, and outputs the rectangular wave signal whose voltage level has been shifted for the benefit of preventing the output voltage from distortion even if the voltage level is low (col. 2 lines 31-34).

Re claim 2, the modified invention as claimed in claim 1, wherein the phase comparator (101) compares the phase of the reference clock signal with the phase of the comparison clock signal on every cycle of the reference clock signal, and produces the rectangular wave signal having three levels, a high voltage level, a low voltage level, and a reference level (fig.5, Nogawa).

Re claim 4, the modified invention as claimed in claim 1, wherein the level shifter (fig.3 (3)) converts three voltage levels ( $V_{ccH}$ ;  $V_{ccL}$  and  $V_{ref}$ ), a voltage level of the rectangular wave signal having the high voltage level (col. 5 lines 1-5), a voltage level of the rectangular wave signal having the low voltage level, and a voltage level of the reference level, to a voltage level for controlling a VCO (fig.4. col. 5 lines 18-29, Chang).

Re claim 6, the modified invention as claimed in claim 1, wherein the phase comparator (101) compares the phase of the reference clock signal with the phase of the comparison clock signal on every cycle of the reference clock signal (fig. col. 6 lines 19-25), and produces the rectangular wave signal having three levels, a high voltage level, a low voltage level, and a reference level (fig.5; col. 7 lines 39-50, lag/lead and

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constant, Nogawa).

Re claim 7, the modified invention as claimed in claim 1, wherein the VCO has an arbitrary voltage-frequency characteristic (col. 4 lines 45-48, Nogawa).

Re claim 8, the modified invention as claimed in claim 1, wherein a mathematical model is used as a principle of operation of the PLL circuit, the mathematical model expressing a response from the PLL circuit by a numeric sequence (equation 1, Nogawa).

5. ***“In re **claims 9-10 and 11** Nogawa in view of Chang discloses an operation analysis and a phase synchronization method for a phase locked loop (PLL) **because under the principles of inherency, if a prior art device, in its normal and usual operation, would necessarily perform the method claims, then the method claimed will be considered to be anticipated by the prior art device. When the prior art device is the same as a device described in the specification for carrying out the claimed method, it can be assumed the device will inherently perform the claimed process. In re King, 801 F.2d 1324,231 MPEP 2112.02”*****

6. **Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nogawa US 6,154,071 in view of Chang et al. US 6,642,769 in further view of Sheir US 4,959,618**

Re claim 5 Chang discloses wherein the level shifter (3) includes: a plurality of resistors connected in series (fig.5c) and controlling a VCO; does not teach a switch that produces VCO the voltage level by switching connections of the plurality of resistors based on the three voltage levels.

However, Shier discloses a switch (22) that produces the voltage level for controlling VCO (16) by switching connections of the plurality of resistors (32,28) based on the three voltage levels (col. 4 lines 16-29).

Therefore, taking the combined teaching of Shier, Nogawa and Chang as a whole would have been rendered obvious to one skilled in the art to modify Nogawa and Chang to switch that produces VCO the voltage level by switching connections of the plurality of resistors based on the three voltage levels for the benefit of matching the frequency output signal of the VCO to the frequency of the incoming data stream (col. 2 lines 58-63, Shier).

### ***Allowable Subject Matter***

7. Claim 3 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims..

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rahel Guarino whose telephone number is (571)270-1198. The examiner can normally be reached on M-F (7:30-4:00).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Payne David can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Rahel Guarino/  
Examiner, Art Unit 2611

/Chieh M Fan/  
Supervisory Patent Examiner, Art Unit 2611